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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,887	11/24/2003	Hsiang Wei Wang	N1085-00224 [TSMC2003-043	5139

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EXAMINER	
ROSASCO, STEPHEN D	

ART UNIT	PAPER NUMBER
1756	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,887	WANG, HSIANG WEI	
	Examiner	Art Unit	
	Stephen Rosasco	1756	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Applicant's election of Group II (claims 1-3) in the reply filed on 8/1/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim (6,487,712).

The claimed invention is directed to a via/contact photomask, comprising a first via/contact pattern serving for forming at least one first functional via/contact plug and a second via/contact pattern serving for forming at least one first dummy via/contact plug within a first dielectric layer, and the first via/contact pattern serving for forming at least one second dummy via/contact plug and the second via/contact pattern serving for forming at least one second functional via/contact plug within a second dielectric layer.

The applicant discusses the limitations of the prior art in that the introduction of the via plug creates a problem, which has been observed in 0.13 um copper technology fabrication. If the photoresist plug is too low, a via facet occurs. The facet is a widening of the via at the top of the lower one of the two dielectric layers, caused by erosion of the via wall near the top of the lower layer. The facet is unacceptable, because, for example, it causes poor deposition of the

TaN barrier layer and copper film in the trench. In order to avoid these problems, it would be desirable to combine various layers, without reducing process efficiencies. And that the contact area would not be appropriate to combine, due to the fact that cell size might be enlarged as a result.

Kim teaches a method of manufacturing a mask for conductive wirings in a semiconductor device, wherein the conductive wirings are formed on a semiconductor substrate of the semiconductor device, comprising the steps of: (a) calculating data for entire regions of the semiconductor substrate on which the conductive wirings are formed; (b) reading size, shape and position of conductive wiring patterns for the conductive wirings to generate data for conductive wirings, and storing the generated conductive wirings data; (c) extending the conductive wirings data by a predetermined size to generate data for extended conductive wirings; (d) subtracting extended conductive wirings data from the data for the entire regions of the semiconductor substrate to calculate a differential data between the extended conductive wirings data and the entire regions data, and to generate data for dummy conductive wiring pattern; (e) adding the conductive wirings data to the dummy conductive wiring pattern data to form a pattern having a size and a position of which correspond to data obtained by an addition operation on the mask by using a clear field method.

wherein the step (d) further comprises a step of subtracting the extended conductive wirings data from the data for the entire regions of the semiconductor substrate to calculate a differential data between the extended conductive wirings data and the entire regions data, and to generate data for a plurality of dummy conductive wiring patterns divided into predetermined

sized regions, each of the predetermined sized regions being spaced apart at a predetermined interval from each other based on the calculated differential data.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. (2003/0044059).

Chang et al. teach a mask for transferring a pattern to an integrated circuit layer, the mask comprising: a plurality of main features; and at least one dummy feature, wherein only the main features reflect post-layout processing.

And wherein the at least one dummy feature provides at least one of mechanical support for the integrated circuit layer, resolution improvement of a main feature for the integrated circuit layer, a test structure for the integrated circuit layer, and a marking for the integrated circuit layer.

And wherein a main feature is distinguished from a dummy feature by combining information from at least two mask layers.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Stephen Rosasco whose telephone number is (571) 272-1389. The Examiner can normally be reached Monday-Friday, from 8:00 AM to 4:30 PM. The Examiner's supervisor, Mark Huff, can be reached on (571) 272-1385. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S. Rosasco
Primary Examiner
Art Unit 1756

S.Rosasco
10/02/05